	L #	Hits	Search Text	DBs
1	L1	4180	(sequenc$3 issu$3 dispatch$3) near10 instruction near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
2	L2	455796	(status state condition) near10 (network rout$3 bus connect$3 interconnect$3 path line)	USPAT; US-PGPUB
3	L3	7078	2 near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
4	L4	522	1 and 3	USPAT; US-PGPUB
5	L5	35351	((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem)).ab,ti.	USPAT; US-PGPUB
6	L6	287	4 and 5	USPAT; US-PGPUB
7	L7	594	(sequenc$3 issu$3 dispatch$3) near10 instruction near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
8	L8	277642	(status state condition) near10 (network rout$3 bus connect$3 interconnect$3 path line)	EPO; JPO; DERWENT; IBM_TDB
9	L9	2470	8 near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
10	L11	15	7 and 9	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 5121502 A	☐	System for selectively communicating instructions from memory locations simultaneously or from the same memory locations sequentially to plurality of processing	712/24
2	US 5121488 A	☐	Sequence controller of an instruction processing unit for placing said unit in a ready, go, hold, or cancel state	712/229
3	US 5109495 A	☒	Method and apparatus using a source operand list and a source operand pointer queue between the execution unit and the instruction decoding and operand processing units of a pipelined data processor	712/207
4	US 5077663 A	☒	Information processing system having microprogram-controlled type arithmetic processing unit with information transfer through a system control unit upon fault detection	714/10
5	US 5067069 A	☒	Control of multiple functional units with parallel operation in a microcoded execution unit	712/218
6	US 5058203 A	☒	Mobile telephone terminal having selectively used processor unit for low power consumption	455/574
7	US 5056015 A	☒	Architectures for serial or parallel loading of writable control store	703/27
8	US 5040108 A	☒	Information processing system having microprogram-controlled type arithmetic processing unit with clock synchronization instruction	709/400
9	US 5038312 A	☒	Data processing system capable of performing vector/matrix processing and arithmetic processing unit incorporated therein	708/520
10	US 5036454 A	☒	Horizontal computer having register multiconnect for execution of a loop with overlapped code	712/241
11	US 5029074 A	☒	Bus adapter unit for digital processing system	710/306
12	US 5021945 A	☒	Parallel processor system for processing natural concurrencies and method therefor	712/216
13	US 5019966 A	☒	Dual processors using busy signal for controlling transfer for predetermined length data when receiving processor is processing previously received data	710/29
14	US 4994724 A	☒	Servo-controlled automatic door having automatic detecting and adjusting mechanism	318/603
15	US 4992933 A	☒	SIMD array processor with global instruction control and reprogrammable instruction decoders	712/22
16	US 4991123 A	☒	Alarm system	340/525
17	US 4991083 A	☒	Method and system for extending address space for vector processing	711/207
18	US 4926320 A	☒	Information processing system having microprogram-controlled type arithmetic processing unit	713/400
19	US 4926317 A	☒	Hierarchical memory system with logical cache, physical cache, and address translation unit for generating a sequence of physical addresses	711/3
20	US 4916695 A	☒	Stored program controlled real time system including three substantially identical processors	714/11
21	US 4891787 A	☒	Parallel processing system with processor array having SIMD/MIMD instruction processing	712/205
22	US 4882702 A	☒	Programmable controller with I/O expansion module located in one of I/O module positions for communication with outside I/O modules	710/2

	Document ID	U	Title	Current OR
23	US 4873626 A	☒	Parallel processing system with processor array having memory system included in system memory	710/120
24	US 4868738 A	☒	Operating system independent virtual memory computer system	710/26
25	US 4847755 A	☒	Parallel processing method and apparatus for increasing processing throughout by parallel processing low level instructions having natural concurrencies	712/203
26	US 4837730 A	☒	Linking scalar results directly to scalar operation inputs on a bidirectional databus in a computer which superpositions vector and scalar operations	712/7
27	US 4817091 A	☒	Fault-tolerant multiprocessor system	714/8
28	US 4816990 A	☒	Method and apparatus for fault-tolerant computer system having expandable processor section	709/400
29	US 4812972 A	☒	Microcode computer having dispatch and main control stores for storing the first and the remaining microinstructions of machine instructions	712/211
30	US 4807116 A	☒	Interprocessor communication	710/113
31	US 4760518 A	☒	Bi-directional databus system for supporting superposition of vector and scalar operations in a computer	710/107
32	US 4750177 A	☒	Digital data processor apparatus with pipelined fault tolerant bus protocol	714/748
33	US 4701847 A	☒	Adaptive instruction sequence synthesizer and process	713/1
34	US 4672537 A	☒	Data error detection and device controller failure detection in an input/output system	714/56
35	US 4672535 A	☒	Multiprocessor system	710/38
36	US 4654857 A	☒	Digital data processor with high reliability	714/5
37	US 4646245 A	☒	Modular installation for assembling and/or machining parts, with work stations including keyboard-display devices	700/113
38	US 4639864 A	☒	Power interlock system and method for use with multiprocessor systems	714/14
39	US 4621360 A	☒	Control method of data transfer	370/438
40	US 4620275 A	☒	Computer system	712/6
41	US 4597084 A	☒	Computer memory apparatus	714/805
42	US 4583160 A	☒	Priority control apparatus for a bus in a bus control system having input/output devices	710/107
43	US 4550368 A	☒	Instruction buffer associated with a cache memory unit	712/200
44	US 4533833 A	☒	Control state sequencer	711/103
45	US 4519028 A	☒	CPU with multi-stage mode register for defining CPU operating environment including charging its communications protocol	713/600

	Document ID	U	Title	Current OR
46	US 4510565 A	☒	Programmable controller with intelligent positioning I/O modules	700/7
47	US 4509116 A	☒	Special instruction processing unit for data processing system	710/105
48	US 4486826 A	☒	Computer peripheral control apparatus	714/9
49	US 4484275 A	☒	Multiprocessor system	710/40
50	US 4453215 A	☒	Central processing apparatus for fault-tolerant computing	714/11
51	US 4451882 A	☒	Data processing system	712/32
52	US 4443865 A	☒	Processor module for a programmable controller	712/242
53	US 4395758 A	☒	Accelerator processor for a data processing system	712/34
54	US 4381542 A	☒	System for interrupt arbitration	710/264
55	US 4373179 A	☒	Dynamic address translation system	711/207
56	US 4365295 A	☒	Multiprocessor system	711/206
57	US 4356550 A	☒	Multiprocessor system	714/14
58	US 4347563 A	☒	Industrial control system	700/8
59	US 4339794 A	☒	Method and system for controlling input/output in process control	710/52
60	US 4313160 A	☒	Distributed input/output controller system	710/23
61	US 4284847 A	☒	Microprocessor-based programmable logic controller	712/248
62	US 4270197 A	☒	Multiprocessor system with demand assignable program paging stores	711/119
63	US 4229790 A	☒	Concurrent task and instruction processor and method	718/101
64	US 4228496 A	☐	Multiprocessor system	710/100
65	US 4179736 A	☐	Microprogrammed computer control unit capable of efficiently executing a large repertoire of instructions for a high performance data processing unit	712/232
66	US 4124889 A	☐	Distributed input/output controller system	710/2
67	US 4124888 A	☐	Peripheral-unit controller apparatus	710/8
68	US 4113989 A	☐	Electronic telephone system featuring switching networks having thyristors for single-wire switching	379/257

	Document ID	U	Title	Current OR
69	US 41058 76 A	☐	Electronic telephone system featuring periodic scanning of all peripheral units and polling of specific peripheral units for transmission of status and/or instruction information	379/257
70	US 41058 75 A	☐	Electronic telephone switching system comprising a speech-path switching matrix and tone-connecting matrix and employing electronic crosspoint switching devices	379/16
71	US 41058 74 A	☐	Centrally controlled electronic telephone system having a customer memory for storing information on two or more different subscriber stations and peripheral equipment-specific information	379/257
72	US 41058 73 A	☐	Electronic telephone switching system comprising a speech path switching matrix and tone-connecting switching matrix and employing electronic crosspoint switches	379/257
73	US 41058 72 A	☐	Electronic telephone system including interexchange trunk repeaters for traffic with other systems	379/257
74	US 41058 71 A	☐	Electronic telephone system featuring a customer memory within a central control unit connected by bus lines	379/280
75	US 41006 01 A	☐	Multiplexer for a distributed input/out controller system	710/32
76	US 40992 41 A	☐	Apparatus for facilitating a cooperation between an executive computer and a reserve computer	709/400
77	US 40806 49 A	☐	Balancing the utilization of I/O system processors	710/48
78	US 40457 82 A	☐	Microprogrammed processor system having external memory	710/5
79	US 40443 33 A	☐	Data processing switching system	710/316
80	US 40245 07 A	☐	Arrangement for monitoring the state of memory segments	711/170
81	US 40245 05 A	☐	Interface system for coupling an indeterminate number of peripheral devices to a central processing unit	710/2
82	US 40152 42 A	☐	Device for coupling several data processing units to a single memory	718/103
83	US 39797 28 A	☐	Array processors	712/16
84	US 38738 19 A	☐	Apparatus and method for fault-condition signal processing	714/47
85	US 38368 89 A	☐	PRIORITY INTERRUPTION CIRCUITS FOR DIGITAL COMPUTER SYSTEMS	710/264
86	US 38052 45 A	☐	I/O DEVICE ATTACHMENT FOR A COMPUTER	710/62
87	US 37019 76 A	☐	FLOATING POINT ARITHMETIC UNIT FOR A PARALLEL PROCESSING COMPUTER	708/209
88	US 36465 23 A	☐	COMPUTER	717/143
89	US 36147 40 A	☐	DATA PROCESSING SYSTEM WITH CIRCUITS FOR TRANSFERRING BETWEEN OPERATING ROUTINES, INTERRUPTION ROUTINES AND SUBROUTINES	712/228

	Document ID	U	Title	Current OR
1	JP 11163087 A	☐	SUBSTRATE PROCESSING DEVICE AND TRANSPORTATION SCHEDULING METHOD	
2	JP 01013628 A	☐	BRANCH CONDITION DETERMINING DEVICE	
3	JP 54107235 A	☐	INTERRUPT CONTROL SYSTEM	
4	EP 1182544 A2	☐	Multiprocessor system with multiple instruction sources	
5	EP 404559 A2	☐	Multiprocessor system with multiple instruction sources.	
6	WO 2003010681 A	☐	System for digital signal processing within an adaptive computing engine has status network for routing status word data resulting from instruction execution in set of composite blocks	
7	WO 2002008859 A	☐	Code translator for central processing unit of programmable computing system, translates instruction from both sequential and target paths of conditional branch instruction	
8	US 6094715 A	☐	Array processing system for business applications, includes processing elements which execute single instruction stream independently of fixed time relationship between processing elements	
9	JP 09198236 A	☐	Instruction sequence decision method for forming source program from flowchart - involves detecting graphic data of functional block linked to next block and stored in second buffer	
10	US 5428811 A	☐	Interface between register file for arbitrating between single and multiple cycle instruction execution co-processor functional units - asserts execution unit write line, between single and multiple cycle units, when single cycle unit requests access to destination bus, and uses arbitration system in multiple cycle unit to prevent bus access when certain lines are asserted	
11	US 5361389 A	☐	Emulation routine instruction issue system - issues each host instruction required in emulation of source instruction program to CPU and uses virtual program counter to indicate address of next host instruction to be executed	
12	EP 519509 A	☐	Woofer loudspeaker module for use in television set - has enclosure with front and rear passages from woofer to open ends with rear passage having upstream expansion and downstream regions	
13	DE 4010311 A	☐	Data processor with interrupt control - allows interruption of central processing unit in response to direct memory access command	
14	WO 8603038 A	☐	Instruction flow computer - includes network which interconnects process control unit with function units and memory units with parallel program execution	
15	GB 2142507 A	☐	Data transfer controlling method for picture processor - using gate circuit to detect coincidence of data send and accept ready states in two operation modules	

	Document ID	U	Title	Current OR
1	US 20040054872 A1	☐	High-performance, superscalar-based computer system with out-of-order intstruction execution	712/206
2	US 20040039952 A1	☒	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/300
3	US 20040025182 A1	☒	Method, system and computer readable medium for a raido communication processing unit	725/61
4	US 20040024938 A1	☒	Flexible interrupt handling methods for optical networking apparatuses with multiple multi-protocol optical networking modules	710/260
5	US 20040015654 A1	☒	Storage subsystem, information processing system and method of controlling I/O interface	711/113
6	US 20030231633 A1	☒	Router apparatus	370/395.31
7	US 20030200539 A1	☒	Function unit based finite state automata data structure, transitions and methods for making the same	717/161
8	US 20030200378 A1	☒	Providing a register file memory with local addressing in a SIMD parallel processor	711/1
9	US 20030196197 A1	☒	Methods and systems for integrated scheduling and resource management for a compiler	717/161
10	US 20030179927 A1	☒	Image processing apparatus and image processing method	382/173
11	US 20030079113 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/205
12	US 20030070060 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
13	US 20030056134 A1	☒	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
14	US 20030056087 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
15	US 20030056086 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
16	US 20030031172 A1	☒	TCP receiver acceleration	370/389
17	US 20030028750 A1	☒	Method and system for digital signal processing in an adaptive computing engine	712/10

	Document ID	U	Title	Current OR
18	US 20030028320 A1	☒	Navigation apparatus	701/210
19	US 20030009643 A1	☒	Two-stage request protocol for accessing remote memory data in a NUMA data processing system	711/155
20	US 20030009634 A1	☒	Non-uniform memory access (NUMA) data processing system that provides notification of remote deallocation of shared data	711/141
21	US 20030009632 A1	☒	Method and system for prefetching utilizing memory initiated prefetch write operations	711/137
22	US 20030009623 A1	☒	Non-uniform memory access (NUMA) data processing system having remote memory cache incorporated within system memory	711/119
23	US 20020181479 A1	☒	Protection system, virtual concatenation processing block, node and ring network	370/404
24	US 20020181392 A1	☒	Protection system, layer 2 function block, node and ring network enabling wideband transmission of working traffic and protection of protection channel traffic	370/216
25	US 20020169969 A1	☒	Information processing unit having tamper - resistant system	713/190
26	US 20020152366 A1	☒	Parallel computer with improved access to adjacent processor and memory elements	712/11
27	US 20020144086 A1	☒	Multiprocessor system. multiprocessor control method, and multiprocessor control program retaining computer-readable recording medium	712/35
28	US 20020133784 A1	☒	Automatic design of VLIW processors	716/1
29	US 20020133260 A1	☒	Operating method of vacuum processing system and vacuum processing system	700/121
30	US 20020133257 A1	☒	Operating method of vacuum processing system and vacuum processing system	700/117
31	US 20020133256 A1	☒	Operating method of vacuum processing system and vacuum processing system	700/117
32	US 20020120914 A1	☒	Automatic design of VLIW processors	716/17
33	US 20020112129 A1	☒	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with store-through data cache	711/141
34	US 20020112124 A1	☒	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with write-back data cache	711/122

	Document ID	U	Title	Current OR
35	US 20020 08329 6 A1	☒	PARALLEL COMPUTER WITH IMPROVED ACCESS TO ADJACENT PROCESSOR AND MEMORY ELEMENTS	712/11
36	US 20020 07828 5 A1	☒	Reduction of interrupts in remote procedure calls	710/260
37	US 20020 05298 5 A1	☒	Storage subsystem, information processing system and method of controlling I/O interface	710/5
38	US 20020 04042 8 A1	☒	Computer system and method of controlling computation	712/225
39	US 20020 03776 9 A1	☒	Game system, storage medium, and entertainment apparatus	463/31
40	US 20020 03068 7 A1	☒	Memory access methods in a unified memory system	345/534
41	US 20020 02932 8 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
42	US 20020 01690 3 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
43	US 20020 01681 5 A1	☒	Web function block in automation equipment	709/203
44	US 20010 03624 2 A1	☒	In-core fixed nuclear instrumentation system and power distribution monitoring system	376/245
45	US 20010 01873 3 A1	☒	Array-type processor	712/16
46	US 66842 86 B1	☒	High-speed block transfer circuit	710/307
47	US 66752 85 B1	☒	Geometric engine including a computational module without memory contention	712/201
48	US 66751 87 B1	☒	Pipelined linear array of processor elements for performing matrix computations	708/622
49	US 66717 67 B2	☒	Storage subsystem, information processing system and method of controlling I/O interface	711/100
50	US 66657 67 B1	☒	Programmer initiated cache block operations	711/3
51	US 66622 75 B2	☒	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with store-through data cache	711/141
52	US 66512 22 B2	☒	Automatic design of VLIW processors	716/1
53	US 66474 85 B2	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23

	Document ID	U	Title	Current OR
54	US 6633959 B2	☒	Non-uniform memory access (NUMA) data processing system that provides notification of remote deallocation of shared data	711/141
55	US 6629312 B1	☒	Programmatic synthesis of a machine description for retargeting a compiler	717/136
56	US 6625659 B1	☒	Router switches to old routing table when communication failure caused by current routing table and investigates the cause of the failure	709/239
57	US 6618777 B1	☒	Method and apparatus for communicating between multiple functional units in a computer environment	710/120
58	US 6615322 B2	☒	Two-stage request protocol for accessing remote memory data in a NUMA data processing system	711/145
59	US 6604190 B1	☒	Data address prediction structure and a method for operating the same	712/207
60	US 6581187 B2	☒	Automatic design of VLIW processors	716/1
61	US 6574714 B2	☒	Efficient instruction cache coherency maintenance mechanism for scalable multiprocessor computer system with write-back data cache	711/141
62	US 6567934 B1	☒	Method and apparatus for verifying multiprocessing design in a unit simulation environment	714/33
63	US 6507947 B1	☒	Programmatic synthesis of processor element arrays	717/160
64	US 6496940 B1	☒	Multiple processor system with standby sparing	714/4
65	US 6490716 B1	☒	Automated design of processor instruction units	716/18
66	US 6421772 B1	☒	Parallel computer with improved access to adjacent processor and memory elements	712/11
67	US 6408041 B2	☒	In-core fixed nuclear instrumentation system and power distribution monitoring system	376/254
68	US 6393546 B1	☒	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
69	US 6385757 B1	☒	Auto design of VLIW processors	716/1
70	US 6374333 B1	☒	Cache coherency protocol in which a load instruction hint bit is employed to indicate deallocation of a modified cache line supplied by intervention	711/145
71	US 6327641 B1	☒	Method of implementing a geometry per wedge (GPW) based headerless solution in a disk drive formatter and a computer program product incorporating the same	711/112
72	US 6310929 B1	☒	In-core fixed nuclear instrumentation system and power distribution monitoring system	376/245
73	US 6282630 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
74	US 6282583 B1	☒	Method and apparatus for memory access in a matrix processor computer	709/400
75	US 6279101 B1	☒	Instruction decoder/dispatch	712/215
76	US 6272619 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41

	Document ID	U	Title	Current OR
77	US 6269279 B1	☒	Control system	700/121
78	US 6266763 B1	☒	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
79	US 6256720 B1	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
80	US 6253313 B1	☒	Parallel processor system for processing natural concurrencies and method therefor	712/226
81	US 6247106 B1	☒	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	711/203
82	US 6247093 B1	☒	Data processing apparatus for executing synchronous instructions prior to executing asynchronous instructions	710/263
83	US 6233702 B1	☒	Self-checked, lock step processor pairs	714/48
84	US 6230262 B1	☒	Processor configured to selectively free physical registers upon retirement of instructions	712/244
85	US 6182203 B1	☒	Microprocessor	712/22
86	US 6157967 A	☒	Method of data communication flow control in a data processing system using busy/ready commands	710/19
87	US 6151689 A	☒	Detecting and isolating errors occurring in data communication in a multiple processor system	714/49
88	US 6148391 A	☒	System for simultaneously accessing one or more stack elements by multiple functional units using real stack addresses	712/202
89	US 6134651 A	☒	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
90	US 6128723 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
91	US 6122656 A	☒	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	718/100
92	US 6119223 A	☒	Map unit having rapid misprediction recovery	712/244
93	US 6115036 A	☒	Video game/videographics program editing apparatus with program halt and data transfer features	345/723
94	US 6108763 A	☒	Simultaneous parity generating/reading circuit for massively parallel processing systems	712/10
95	US 6101594 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
96	US 6094715 A	☒	SIMD/MIMD processing synchronization	712/20
97	US 6092181 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
98	US 6085271 A	☒	System bus arbitrator for facilitating multiple transactions in a computer system	710/113

	Document ID	U	Title	Current OR
99	US 6079008 A	☒	Multiple thread multiple data predictive coded parallel processing system and method	712/11
100	US 6079006 A	☒	Stride-based data address prediction structure	711/213
101	US 6070235 A	☒	Data processing system and method for capturing history buffer data	712/23
102	US 6047248 A	☒	Performance-temperature optimization by cooperatively varying the voltage and frequency of a circuit	702/132
103	US 6038654 A	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
104	US 6038653 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
105	US 6038644 A	☒	Multiprocessor system with partial broadcast capability of a cache coherent processing request	711/141
106	US 6038585 A	☒	Autonomous distributed instruction book control device	718/100
107	US 6032252 A	☒	Apparatus and method for efficient loop control in a superscalar microprocessor	712/233
108	US 6014741 A	☒	Apparatus and method for predicting an end of a microcode loop	712/233
109	US 5996083 A	☒	Microprocessor having software controllable power consumption	713/322
110	US 5974565 A	☒	Composite computer system	714/11
111	US 5974537 A	☒	Guard bits in a VLIW instruction control routing of operations to functional units allowing two issue slots to specify the same functional unit	712/215
112	US 5968167 A	☒	Multi-threaded data processing management system	712/225
113	US 5968160 A	☒	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	712/14
114	US 5968159 A	☒	Interrupt system with fast response time	710/264
115	US 5966528 A	☒	SIMD/MIMD array processor with vector processing	712/222
116	US 5964835 A	☒	Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source	709/216
117	US 5961629 A	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
118	US 5953535 A	☒	Using intelligent bus bridges with pico-code to service interrupts and improve interrupt response	710/260
119	US 5951628 A	☒	Method and system for performing a convolution operation	708/420
120	US 5940928 A	☒	Surface maintenance machine with computer controlled operational and maintenance systems	15/319
121	US 5940785 A	☒	Performance-temperature optimization by cooperatively varying the voltage and frequency of a circuit	702/132

	Document ID	U	Title	Current OR
122	US 5936871 A	☒	Method and system for performing an L.sub.2 norm operation	708/517
123	US 5923890 A	☒	Method and apparatus for optimizing the handling of synchronous requests to a coupling facility in a sysplex configuration	712/1
124	US 5920710 A	☒	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
125	US 5914953 A	☒	Network message routing using routing table information and supplemental enable information for deadlock prevention	370/392
126	US 5905581 A	☒	Image forming apparatus	358/468
127	US 5903772 A	☒	Plural operand buses of intermediate widths coupling to narrower width integer and wider width floating point superscalar processing core	712/33
128	US 5898865 A	☒	Apparatus and method for predicting an end of loop for string instructions	712/239
129	US 5881265 A	☒	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/218
130	US 5878241 A	☒	Partitioning of processing elements in a SIMD/MIMD array processor	712/203
131	US 5870619 A	☒	Array processor with asynchronous availability of a next SIMD instruction	712/20
132	US 5870579 A	☒	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
133	US 5854921 A	☒	Stride-based data address prediction structure	712/239
134	US 5838894 A	☒	Logical, fail-functional, dual central processor units formed from three processor units	714/11
135	US 5832292 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
136	US 5828860 A	☒	Data processing device equipped with cache memory and a storage unit for storing data between a main storage or CPU cache memory	712/207
137	US 5828859 A	☒	Method and apparatus for setting the status mode of a central processing unit	712/200
138	US 5822574 A	☒	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
139	US 5815715 A	☒	Method for designing a product having hardware and software components and product therefor	717/141
140	US 5812757 A	☒	Processing board, a computer, and a fault recovery method for the computer	714/11
141	US 5794067 A	☒	Digital signal processing device	712/35
142	US 5790776 A	☒	Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements	714/10
143	US 5784630 A	☒	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	712/30
144	US 5768553 A	☒	Microprocessor using an instruction field to define DSP instructions	712/208

	Document ID	U	Title	Current OR
145	US 5765037 A	☒	System for executing instructions with delayed firing times	713/502
146	US 5765011 A	☒	Parallel processing system having a synchronous SIMD processing with processing elements emulating SIMD operation using individual instruction streams	712/20
147	US 5764938 A	☒	Resynchronization of a superscalar processor	712/200
148	US 5764076 A	☒	Circuit for partially reprogramming an operational programmable logic device	326/38
149	US 5761523 A	☒	Parallel processing system having asynchronous SIMD processing and data parallel coding	712/20
150	US 5754871 A	☒	Parallel processing system having asynchronous SIMD processing	712/20
151	US 5752067 A	☒	Fully scalable parallel processing system having asynchronous SIMD processing	712/16
152	US 5751955 A	☒	Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory	714/12
153	US 5751932 A	☒	Fail-fast, fail-functional, fault-tolerant multiprocessor system	714/12
154	US 5751760 A	☒	Controller for a telephone system with code screening of incoming calls	379/211.01
155	US 5748516 A	☒	Floating point processing unit with forced arithmetic results	708/497
156	US 5737629 A	☒	Dependency checking and forwarding of variable width operands	712/23
157	US 5729758 A	☒	SIMD processor operating with a plurality of parallel processing elements in synchronization	712/22
158	US 5717944 A	☒	Autonomous SIMD/MIMD processor memory elements	712/20
159	US 5713037 A	☒	Slide bus communication functions for SIMD/MIMD array processor	702/33
160	US 5708836 A	☒	SIMD/MIMD inter-processor communication	712/20
161	US 5708795 A	☒	Asynchronous access system for multiprocessor system and processor module used in the asynchronous access system	711/167
162	US 5699536 A	☒	Computer processing system employing dynamic instruction formatting	712/216
163	US 5699460 A	☒	Image compression coprocessor with data flow control and multiple processing units	382/307
164	US 5694584 A	☒	Information processing system capable of quickly processing a parameter and a command necessary for drawing processing	345/553
165	US 5689720 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution	712/23
166	US 5689689 A	☒	Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal	709/400

	Document ID	U	Title	Current OR
167	US 5682492 A	☒	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/214
168	US 5680534 A	☒	Video game/videographics program fabricating system and method with superimpose control	345/473
169	US 5680533 A	☒	Videographics program/video game fabricating system and method	345/473
170	US 5675807 A	☒	Interrupt message delivery identified by storage location of received interrupt data	710/260
171	US 5655131 A	☒	SIMD architecture for connection to host processor's bus	712/34
172	US 5649225 A	☒	Resynchronization of a superscalar processor	712/23
173	US 5642479 A	☒	Trace analysis of data processing	714/45
174	US 5592609 A	☒	Video game/videographics program fabricating system and method with unit based program processing	345/473
175	US 5590352 A	☒	Dependency checking and forwarding of variable width operands	712/23
176	US 5590348 A	☒	Status predictor for combined shifter-rotate/merge unit	712/223
177	US 5574928 A	☒	Mixed integer/floating point processor core for a superscalar microprocessor with a plurality of operand buses for transferring operand segments	712/23
178	US 5560032 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
179	US 5553276 A	☒	Self-time processor with dynamic clock generator having plurality of tracking elements for outputting sequencing signals to functional units	713/500
180	US 5532828 A	☒	Accelerated interface between processors and hardware adapters	345/501
181	US 5420957 A	☒	Method for controlling vector data execution	712/222
182	US 5399911 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
183	US 5220658 A	☒	Distributed shared-memory multiprocessor system with reduced traffic on shared bus	711/145
184	US 5450603 A	☒	SIMD architecture with transfer register or value source circuitry connected to bus	712/22
185	US 5442757 A	☒	Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts	712/218
186	US 5428811 A	☒	Interface between a register file which arbitrates between a number of single cycle and multiple cycle functional units	712/23
187	US 5418970 A	☒	Parallel processing system with processor array with processing elements addressing associated memories using host supplied address value and base register content	712/20
188	US 5404541 A	☒	Operation monitoring and controlling apparatus for computer system	713/324
189	US 5361389 A	☒	Apparatus and method for emulation routine instruction issue	703/27

	Document ID	U	Title	Current OR
190	US 5353428 A	☒	Information processing apparatus in which a cache memory can be operated in both store-in and store-through modes	711/145
191	US 5321830 A	☒	Reset method when adaptor module is faulty and computer system executing same	714/23
192	US 5276819 A	☒	Horizontal computer having register multiconnect for operand address generation during execution of iterations of a loop of program code	711/214
193	US 5268856 A	☒	Bit serial floating point parallel processing system and method	708/514
194	US 5226128 A	☒	Horizontal computer having register multiconnect for execution of a loop with a branch	712/241
195	US 5226126 A	☒	Processor having plurality of functional units for orderly retiring outstanding operations based upon its associated tags	712/218
196	US 5202887 A	☒	Access control method for shared duplex direct access storage device and computer system therefor	714/8
197	US 5165023 A	☒	Parallel processing system with processor array and network communications system for transmitting messages of variable length	710/317
198	US 5129092 A	☒	Linear chain of parallel processors and method of using same	712/16
199	US 5121502 A	☒	System for selectively communicating instructions from memory locations simultaneously or from the same memory locations sequentially to plurality of processing	712/24
200	US 5121488 A	☐	Sequence controller of an instruction processing unit for placing said unit in a ready, go, hold, or cancel state	712/229